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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/849,885	05/02/2001	Jason Seung-Min Kim	2100653-991350	9967

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EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/849,885	Applicant(s) KIM, JASON SEUNG-MIN	
	Examiner Tim T. Vo	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-40 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-40 are rejected under 35 U.S.C. § **102**(**b**) as being anticipated by Yamada et al. patent number 5,590,380 referred hereinafter "Yamada".

As for claims 1, 12, 23, 31 and 39-40, Yamada teaches a computer system having an interrupt handling apparatus, the computer system comprising:

one or more processors (see figure 1, CPU 2-1 to 2-n);

one or more hardware devices that are capable of interrupting the one or more processors using an interrupt signal (see column 2 lines 56-60 and figure 1, I/O devices I/O 1 to I/Om and column 6 lines 45-53 discloses one or more I/O device generates interrupt to one or more CPU 2-1 to CPU 2-n);

an interrupt controller that is capable of handling the interrupts from the interrupts from the one or more hardware devices and capable of independently generating a low

priority interrupt signal and a high priority interrupt signal for each processor (see figure 1, interrupt controller 4-1 to 4-n and column 8 line 66 to column 8 line 64, wherein each I/O devices generates an interrupt to the each interrupt controller, the interrupt controller then compares the priority interrupt level of each I/O device with the interrupt level set in the corresponding interrupt controller if the interrupt level is higher than the priority level set the interrupt controller routes that interrupt to the corresponding CPU and if the interrupt level is lower than the priority level set the interrupt controller negated that interrupt signal);

the interrupt controller further comprising an enable device that is capable of enabling the interrupt signal independently for each processor and a priority device that is capable of assigning a priority to each interrupt signal destined for any processor wherein a particular interrupt signal is capable of being routed to either processor and is capable is being assigned a low priority or high priority (see figure 1, column 7 line 66 to column 8 line 64, wherein the interrupt controller compares the request priority level from the I/O devices with the priority set in the interrupt controller, if the request priority level is higher than the priority level set, the interrupt controller routes to corresponding CPU other wise if the request priority level is lower than the priority level set, the interrupt controller negated the request).

As for claims 2 and 13, Yamada teaches first processor enable device that is capable of enabling the interrupt signals for the first processor and the a second processor enable device that is capable of enabling the interrupt signals for the second processor (see figure 1, I/O devices generates IR1 to IRm requests and the interrupt

controller examined these request in order to route each individual request signal to a corresponding CPU).

As for claims 3-4, 14-15, 24-25 and 32-33, Yamada teaches each enable device comprises one or more flip-flops connected together with one or more logical gates (see figure 4 and column 4 lines 55-67).

As for claims 5, 16, 27, 30, 35 and 38, Yamada teaches the priority device further comprises a first processor priority device that is capable of assigning a priority to the interrupt signals for the first processor and a second processor priority device that is capable of assigning a priority to the interrupt signals for the second processor (see column 3 lines 32-38).

As for claims 6 and 17, Yamada teaches each priority device comprises one or more flip flops connected together with one or more logical gates (see figure 4 and column 4 lines 55-67).

As for claims 7-9, 18-20, 26, 28-29, 34 and 36-37, Yamada teaches each priority device further comprises a register containing an interrupt priority signal that is fed into the logical gates in order to determine the priority for the interrupt signals of the particular processor (see figure 1, I/O devices generates IR1 to IRm requests, the interrupt controllers determines priority level by comparing its set priority level if the request priority level is higher then that request routes to corresponds CPU otherwise negated the request).

As for claims 10-11 and 21-22, Yamada teaches the interrupt controller further comprises a device for multiplexing the one or more hardware interrupt signals with one

or more software interrupt signals so that the processors are capable of being interrupted by hardware and software (see figure 1 and column 2 lines 51-64).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Tim T. Vo
Examiner
Art Unit 2189

T.V
11/17/03